

FIG. 1

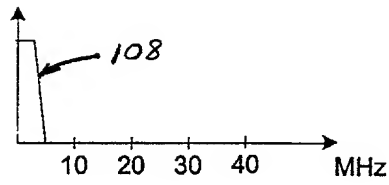


FIG. 2

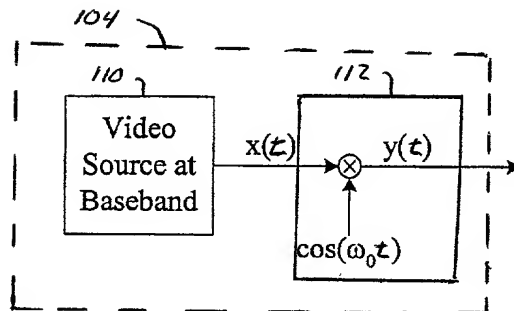


FIG. 3

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FIG. 4A

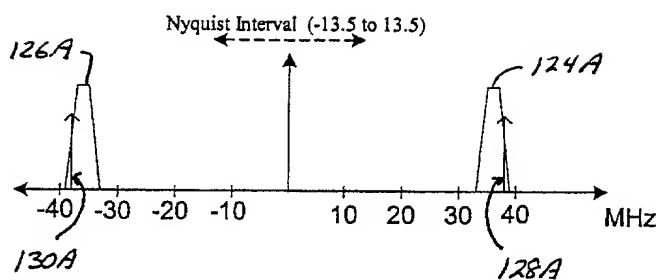


FIG. 4B

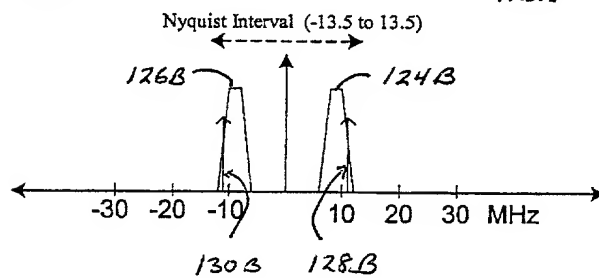


FIG. 5A

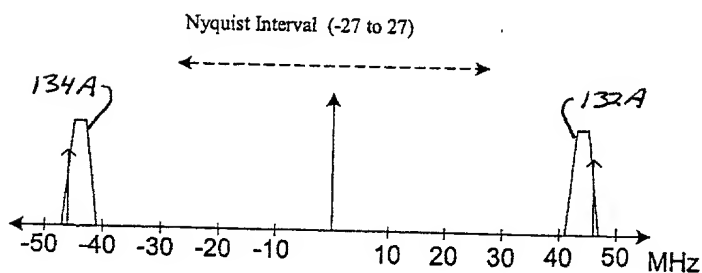
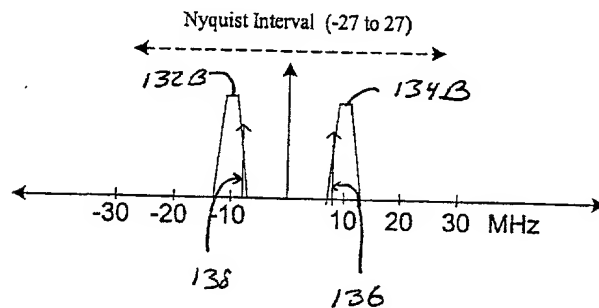


FIG. 5B



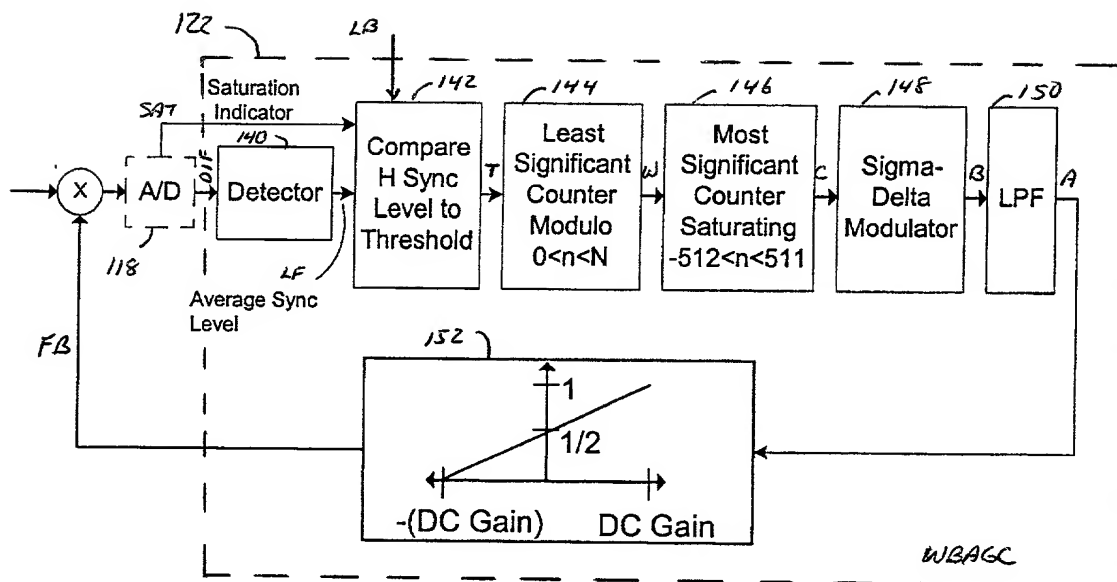


FIG. 6

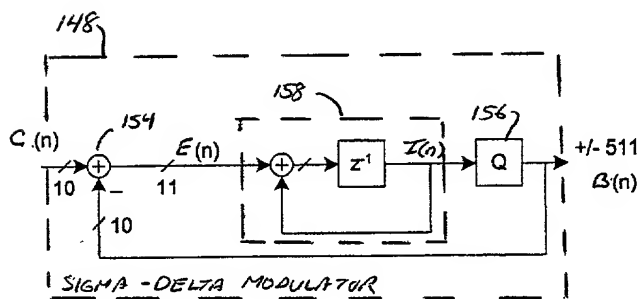


FIG. 7

The diagram illustrates a video detector circuit (140) with the following components and signal paths:

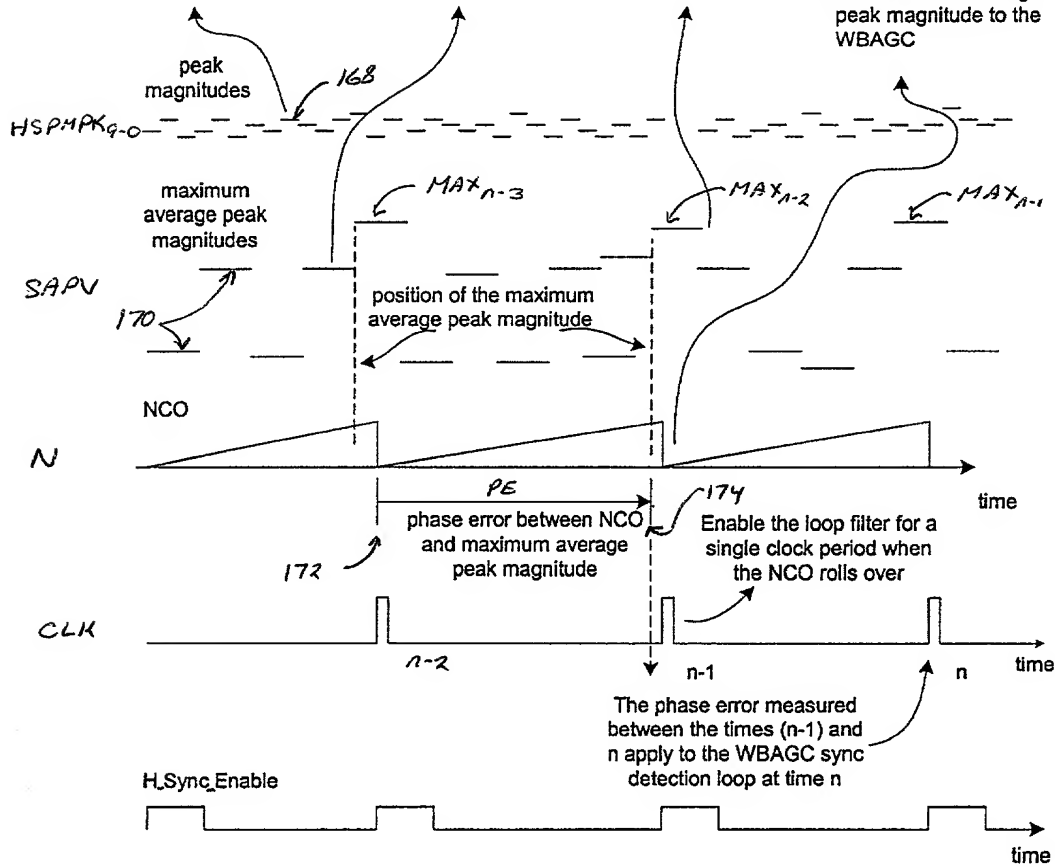
- Inputs:**
 - DIF** (Differential Input Frequency) is connected to the **A/D Output**.
 - Average H Sync Level to WBAGC** is connected to the **Phase and Amplitude Detector** (160).
 - N** (Reference Frequency) is connected to the **Tracking Detector** (166).
- Phase and Amplitude Detector (160):**
 - Outputs a **Phase Error PE** (9 bits) to the **Tracking Detector** (166).
 - Outputs a **LF** (Loop Filter) signal to the **Average H Sync Level to WBAGC**.
- Tracking Detector (166):**
 - Contains a **Direct Gain** block (8 bits) and an **Indirect Gain** block (8 bits).
 - The **Direct Gain** block is followed by a right shift register (**>> 9**) to produce signal **178** (8 bits).
 - The **Indirect Gain** block is followed by a right shift register (**>> 9**) to produce signal **180** (8 bits).
 - Signal **180** is added to the output of a delay block (**z⁻¹**) to produce signal **13** (13 bits).
 - Signal **13** is added to the output of a delay block (**z⁻¹**) to produce signal **11** (11 bits).
 - Signal **11** is added to the output of a delay block (**z⁻¹**) to produce signal **12** (12 bits).
 - Signal **12** is added to the output of a delay block (**z⁻¹**) to produce signal **167** (16 bits).
 - Signal **167** is added to the output of a delay block (**z⁻¹**) to produce signal **24** (24 bits).
 - Signal **24** is added to the output of a delay block (**z⁻¹**) to produce signal **24** (24 bits).
 - Signal **24** is added to the output of a delay block (**z⁻¹**) to produce signal **24** (24 bits).
- Loop Filter (167):**
 - Outputs a signal to the **Tracking Detector** (166).
- Update at NCO rollover:** A signal indicating when the Numerically Controlled Oscillator (NCO) rolls over, connected to the **Tracking Detector** (166).
- NCO (164):**
 - Outputs a signal to the **Tracking Detector** (166).
 - Configured for **PAL: 27 MHz** and **NTSC: 54 MHz**.

166

Tracking Detector

FIG. 9

Find the peak magnitude (HSPMPK ₉₋₀) out of every HSPPKI ₃₋₀ samples	Accumulate the peak magnitudes over every HSPWID ₈₋₀ samples	After every HSPWID ₈₋₀ samples store the position and value of maximum average peak magnitude	When the NCO rolls over apply the phase error to the WBAGC Sync Detector Loop and apply the maximum average
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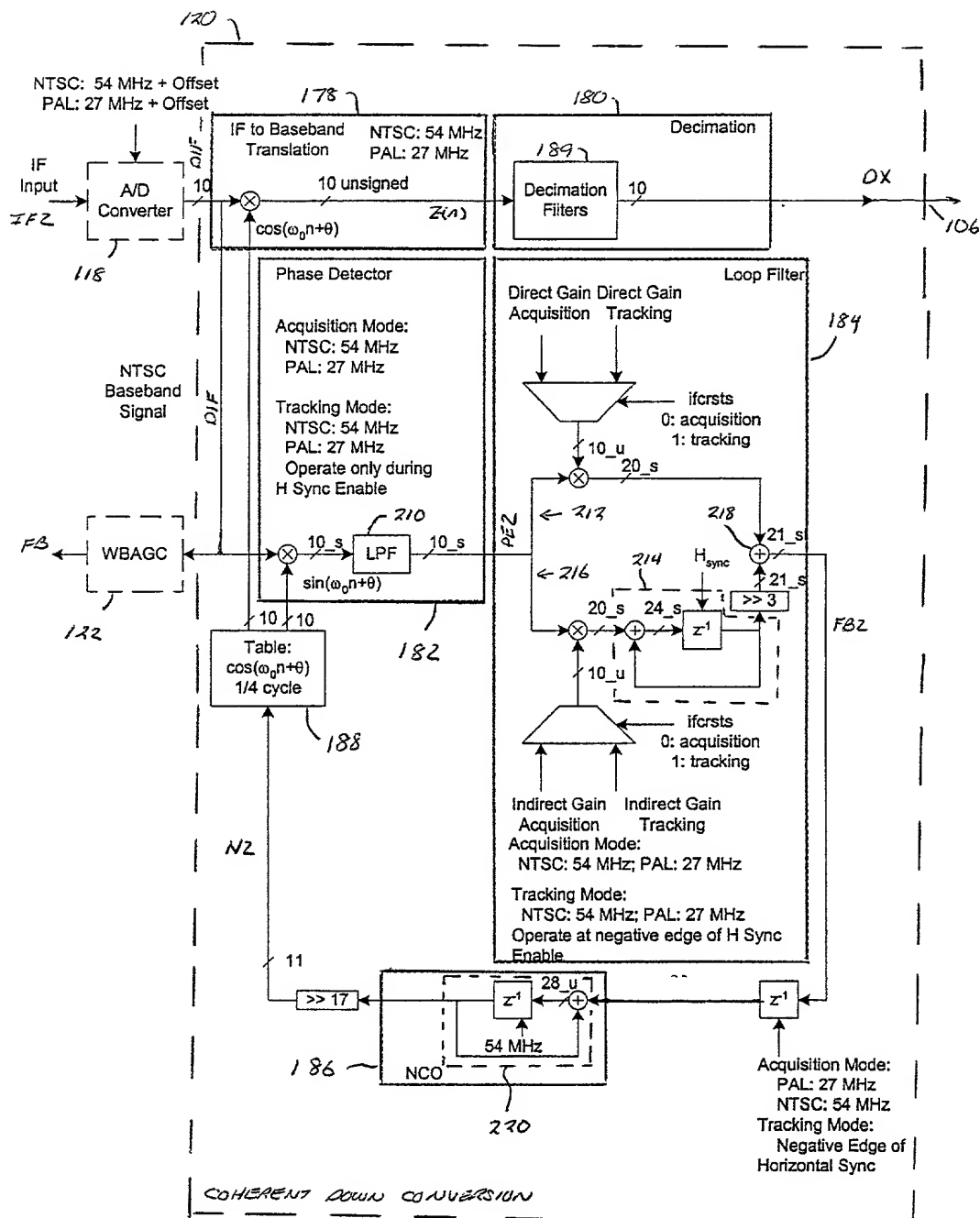


FIG. 11

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FIG. 12

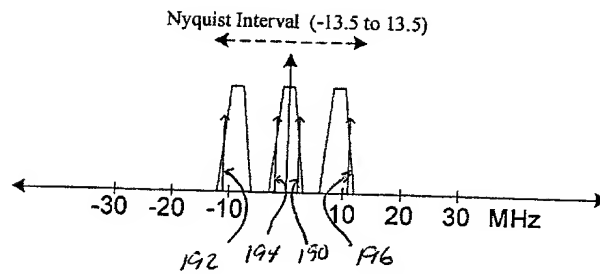


FIG. 13

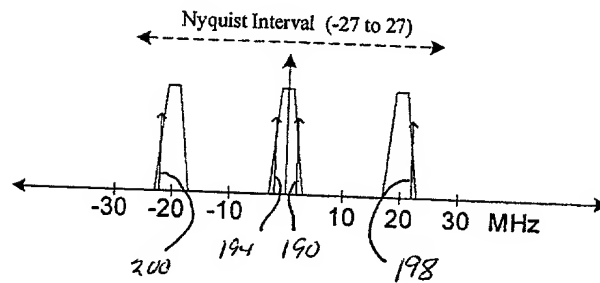


FIG. 14

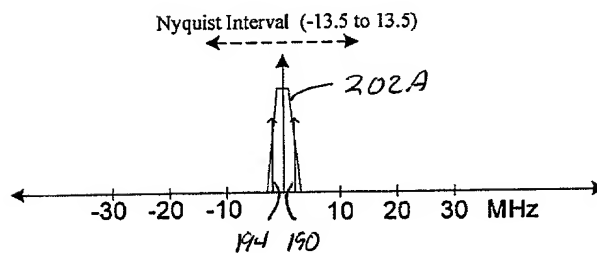
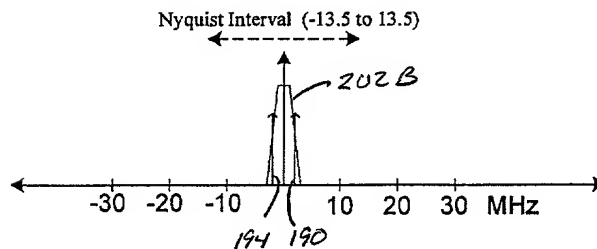


FIG. 15



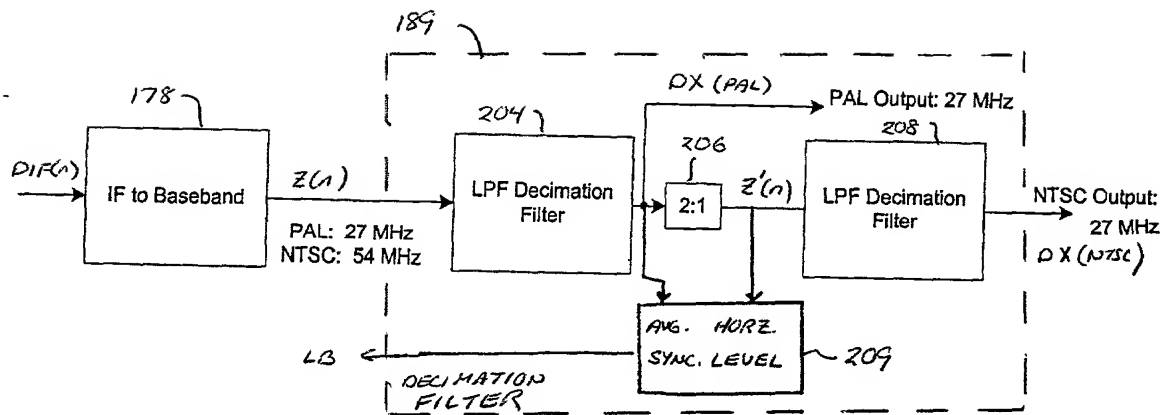


FIG. 16

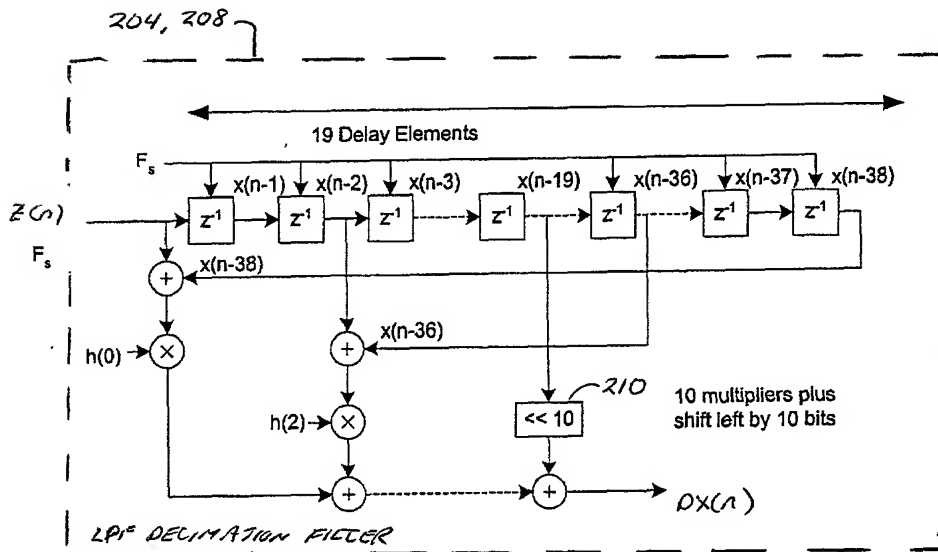


FIG. 17

